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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/632,186	07/30/2003	Yi Ding	M-15241 US	3961

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EXAMINER
NGUYEN, THANH T

ART UNIT	PAPER NUMBER
2813	

DATE MAILED: 07/12/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/632,186	DING, YI	
	Examiner	Art Unit	
	Thanh T. Nguyen	2813	

-- Th MAILING DATE of this communication appears on the cover sh et with th correspond nc address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-19* is/are pending in the application.

4a) Of the above claim(s) *10-19* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,4,7 and 8* is/are rejected.

7)☐ Claim(s) *2-3, 5-6, 9* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/30/03;4/20/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Restriction to one of the following inventions is required under 35 U.S.C. 121:

I. Claims 1-9, drawn to a method for manufacturing an integrated circuit comprising a nonvolatile memory, classified in class 438, subclass 137.

II. Claims 10-19, drawn to an integrated circuit, classified in class 257, subclass 314.

The inventions are distinct, each from the other because of the following reasons:

Inventions I and II are related as process and apparatus for its practice. The inventions are distinct if it can be shown that either: (1) the process as claimed can be practiced by another materially different apparatus or by hand, or (2) the apparatus as claimed can be used to practice another and materially different process. (MPEP § 806.05(e)). In this case the product can be formed by materially different process, for example forming a dielectric layer by thermally grow or chemical vapor deposition process.

Because these inventions are distinct for the reasons given above and have acquired a separate status in the art as shown by their different classification, restriction for examination purposes as indicated is proper.

During a telephone conversation with Michael Shenker on 6/29/04 a provisional election was made with traverse to prosecute the invention of group I, claims 1-9. Affirmation of this election must be made by applicant in replying to this Office action. Claims 10-19 are

withdrawn from further consideration by the examiner, 37 CFR 1.142(b), as being drawn to a non-elected invention.

Information Disclosure Statement

The information disclosure statement filed on 7/30/03 and 4/24/04 has been partially considered because: The information disclosure statement filed 7/30/03 and 4/24/04 fails to comply with 37 CFR 1.98(a)(2), which requires a legible copy of each U.S. and foreign patent; each publication or that portion which caused it to be listed; and all other information or that portion which caused it to be listed. It has been placed in the application file, but the information referred to therein has not been considered.

Oath/Declaration

Oath/Declaration filed on 7/30/03 has been considered.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1, 4, 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by the Admitted Prior Art, Figures 1-9, paragraphs 2-7.

Referring to figures 1-9, the Admitted Prior Art teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

Forming a first structure over a semiconductor substrate (120), the first structure comprising:

A first conductive gate (140, polysilicon) of a nonvolatile memory cell; and

A first dielectric (154, ONO) over the first conductive gate;

Forming a layer (160, "FG layer") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion (160, wherein the first portion is defined as the horizontal portion line between #164 and #154) and an upward protruding second portion, the second portion (160, wherein the second portion is the horizontal portion line above #150 and the vertical portion of the layer 160) being formed over the first dielectric and overlaying a sidewall of the first conductive gate (see figure 9).

Regarding to claim 4, wherein the FG layer consists of one or more sub-layers all of which are present in both the first and the second portions of the floating gates (160, see figure 9).

Regarding to claim 7, the memory cell is one of a plurality of the memory cells, and the method further comprises a masked etch of the FG layer to remove portions of the FG layer between different memory cell (see paragraph 2-4. It is inherent to form more then once memory cell in the wafer and etch by using the mask to form multiple b/c the process would save time).

Regarding to claim 8, forming second conductive gate for the memory cell (170, the upper portion and the lower portion of the conductive layer 170), the second conductive gate being insulated from the first conductive gate and the floating gate (see figure 9, wherein the second conductive gate (170) is being insulated by insulating layer (164) from the first conductive gate and the floating gate, see figure 9).

Claims 1, 4, 7-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Wang (U.S. Patent No. 6,232,185).

Referring to figures 6a-10f, Wang teaches a method for manufacturing an integrated circuit comprising a nonvolatile memory, the method comprising:

Forming a first structure over a semiconductor substrate (91), the first structure comprising:

A first conductive gate (90) of a nonvolatile memory cell; and

A first dielectric (100) over the first conductive gate;

Forming a layer ("FG layer ") to provide at least two conductive floating gates for the memory cell, wherein each floating gate comprises a first portion (130a) and an upward protruding second portion, the second portion (130b) being formed over the first dielectric and overlaying a sidewall of the first conductive gate.

Regarding to claim 4, wherein the FG layer consists of one or more sub-layers all of which are present in both the first and the second portions of the floating gates (130a/130b, see figure 6F).

Regarding to claim 7, the memory cell is one of a plurality of the memory cells (see col. 3, lines 15-16), and the method further comprises a masked (180/190) etch of the FG layer to remove portions of the FG layer between different memory cell. (see figure 6H-6I)

Regarding to claim 8, forming second conductive gate for the memory cell (170, the upper portion and the lower portion of the conductive layer 170), the second conductive gate being insulated from the first conductive gate and the floating gate (see figure 6H, wherein the second conductive gate (170) is being insulated by insulating layer (140) from the first conductive gate and the floating gate, see figure 6H).

Allowable Subject Matter

Claims 2-3, 5-6, 9 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. Since none of the Prior Art taught or suggested the step of the FG layer comprises a first sub-layer and a second sub-layer formed after the first sub-layer, wherein the first portion of each floating gate is formed from the first sub-layer, and the second portion of each floating gate is formed form the second sub-layer.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Thanh Nguyen whose telephone number is (571) 272-1695, or by

Email via address Thanh.Nguyen@uspto.gov. The examiner can normally be reached on Monday-Thursday from 6:00AM to 3:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead, Jr., can be reached on (571) 272-1702. The fax phone number for this Group is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Group receptionist whose telephone number is (703) 308-0956 (**See MPEP 203.08**).

Thanh Nguyen
Patent Examiner
Patent Examining Group 2800

TTN